REMARKS

Amended Claims

Claims 1 and 8 are herein amended.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-30 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Nozoe et al. (U.S. Patent No. 6,351,412). Applicant respectfully traverses this rejection and feels that claims 1-30 are allowable for the following reasons.

In the Final Office Action mailed on April 29, 2005, the Examiner disagreed with Applicant's assertion that Nozoe et al. does not disclose or suggest storing data on the type of defect in the address location (*See*, Final Office Action of April 29, 2005, Page 2). The Examiner asserted, in part, that "[t]he prior art of record, Nozoe teaches (col. 10) the flash memory . . . ," "Where necessary, there may be added a defective address register that retains a address, and a redundancy circuit that replaces a selected memory column with a spare memory portion at the time of an address match. The Examiner would like to point out that the type of defect must be known in order to correct it."

Applicant respectfully disagrees and continues to maintain that Nozoe et al. does not disclose or suggest storing data on the type of defect at the address location it is replacing, but only teaches storing the address of a defective location and then replacing that location when it is accessed with a redundant spare memory column. Applicant therefore maintains that Nozoe et al. merely teaches that to repair a defective location only the address of the defect needs to be stored. *See, e.g.*, Nozoe et al., column 10, lines 32-37.

Applicant therefore respectfully submits that Nozoe et al. does not teach or suggest storing an error code indicating the type of defect of the defective primary memory cells in the array, in addition to storing the address. Applicant thus respectfully submits that Nozoe et al. does not teach or suggest all elements of the Applicant's claimed invention, as maintained by the Examiner.

If the Examiner is maintaining that inherently "the type of defect must be known in order to correct it," and that therefore Nozoe et al. inherently stores data on the type of defect it is repairing in its memory array, the Applicant respectfully disagrees and herein traverses this assertion, maintaining that no such data storage is disclosed or suggested by Nozoe et al. The Applicant notes that Nozoe et al. only states that "[w]here necessary, there may be added a defective address register that retains a location (address) of a defective bit, an address comparator that compares a Y address with a defective address, and a redundancy circuit that replaces a selected memory column with a spare memory portion at the time of an address match." As stated above, Applicant maintains that Nozoe et al. only teaches storing the address of a defective location in a memory array and then replacing that location with a redundant spare memory column when it is accessed. Applicant can find no mention of the storage of data on the type of defect being repaired in Nozoe et al. to support the Examiner's assertion and respectfully requests that a secondary reference or reasoned statement be provided to support the Examiner's assertion. *See, e.g.,* Nozoe et al., Column 10, lines 32-37. Applicant notes that it is well known to those skilled in the art that, in replacing defective elements in prior art memory arrays, only the address(es) affected by the defective memory location, column, or row (and not the defect type) is needed to replace that defective element with a redundant or spare memory element when the defective element is accessed. Applicant respectfully submits that if the Examiner maintains that this an inherent feature, the Examiner has the burden of proving that the inherent element must of necessity only work in the manner of the Applicant's claimed invention. If any other interpretation is possible for the inherent element relied upon for the rejection, the rejection cannot be maintained. "To establish inherency, the extrinsic evidence 'must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill. Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient.'" In re Robertson, 169 F.3d 743, 745, 49 USPQ2d 1949, 1950-51 (Fed. Cir. 1999) (citations omitted); (*See,* MPEP §2112 and §2163.07(a)). Applicant requests that the Examiner state the rational or evidence supporting this assertion as the Examiner is required to do in MPEP §2112. "In relying upon the theory of inherency, the examiner must provide a basis in fact and/or technical reasoning to reasonably support the

determination that the allegedly inherent characteristic necessarily flows from the teachings of the applied prior art." Ex parte Levy, 17 USPQ2d 1461, 1464 (Bd. Pat. App. & Inter. 1990) (emphasis in original). *See*, MPEP §2112.

If, alternatively, the Examiner is taking Official Notice of the fact that "the type of defect must be known in order to correct it" (or, stated otherwise, that to repair a defect in a memory array its type must be known), the Applicant herein traverses this assertion and requests that the Examiner cite to a reference or provide reasoning in support of this position, as the Examiner is required to do by MPEP §2144.03. The Applicant notes that sufficient information or argument was given in the Applicant's above arguments to create on its face a reasonable doubt regarding the circumstances justifying any official notice by the Examiner regarding this matter.

The Applicant maintains that therefore for the reasons listed above in regards to anticipation with explicit or inherent elements, that any taking of official notice is herein rebutted and that claims 1-30 are therefore deemed allowable.

In addition to the above arguments, the Applicant further contends that there is no motivation or suggestion to modify the reference, Nozoe et al., in this manner. Specifically, Applicant contends that to modify Nozoe et al. to provide storage of defect types would require a modification of Nozoe et al.'s defective address register to allow storage of defect type as well as the defect address location. Nozoe et al. expressly teaches away from this and only states that the "defect register retains a location (address) of a defective bit." *See, e.g.*, Nozoe et al., column 10, lines 32-37. Applicant also finds no motivation or suggestion to modify the operation of Nozoe et al. expressly or impliedly contained in the Nozoe et al. reference, and the Office Action does not provide a convincing line of reasoning as to why an artisan would have found the claimed invention to have been obvious in light of the teachings of the reference. Applicant thus submits that the Office has failed to meet its burden of establishing a *prima facie* case of obviousness. *See* MPEP § 706.02(j) ("The initial burden is on the examiner to provide some suggestion of the desirability of doing what the inventor has done. 'To support the conclusion that the claimed invention is directed to obvious subject matter, either the references must expressly or impliedly suggest the claimed invention or the examiner must present a convincing line of reasoning as to why the artisan would have found the claimed invention to have been obvious in light of the teachings of the references.'").

Applicant's claim 1 recites, in part, "redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect in addition to a defect location." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having redundant fuse circuitry used to replace the primary memory cells with the redundant memory cells, wherein the redundant fuse circuitry stores an error code indicating a type of defect. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 1.

Applicant's claim 8 recites, in part, "at least one register to store an address of a defective element in a primary memory array, the register having at least one data bit to store an error code in addition to a defect location." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having at least one register to store an address of a defective element in a primary memory array, the register having at least one data bit to store an error code. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 8.

Applicant's claim 12 recites, in part, "a register for each redundant array element to store an address of a defective element in the memory array, each register further stores an error code." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a register for each redundant array element to store an address of a defective element in the memory array, each register further stores an error code. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 12.

Applicant's claim 17 recites, in part, "a register for each redundant row to store the address of the associated defective row, each register further stores an error code, wherein the error code indicates the type of error the redundant row is used to correct." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a register for each redundant row to store the address of the associated defective row, each register further stores an error code, wherein the error code indicates the type of error the redundant row is used to correct. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 17.

Applicant's claim 20 recites, in part, "a register for each redundant column to store the address of the associated defective column, each register having at least one extra bit to store an error code, wherein the error code indicates the type of error in the at least one defective

column." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a register for each redundant column to store the address of the associated defective column, each register having at least one extra bit to store an error code, wherein the error code indicates the type of error in the at least one defective column. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 20.

Applicant's claim 24 recites, in part, "a register for each redundant row to store the address of an associated defective row, each register further having at least one bit to store an error code, wherein the error code indicates the type of defect in the associated defective row." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a register for each redundant row to store the address of an associated defective row, each register further having at least one bit to store an error code, wherein the error code indicates the type of defect in the associated defective row. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 24.

Applicant's claim 28 recites, in part, "a register for each redundant row and each redundant column to store the addresses of associated defective rows and columns, each register having at least one bit to store an error code, wherein the error code indicates the type of defect the redundant row or column is used to correct." As detailed above, Applicant submits that Nozoe et al. fails to teach or suggest such a flash memory device having a register for each redundant row and each redundant column to store the addresses of associated defective rows and columns, each register having at least one bit to store an error code, wherein the error code indicates the type of defect the redundant row or column is used to correct. As such, Nozoe et al. fails to teach or suggest all elements of independent claim 28.

Applicant respectfully contends that the Examiner has not met the burden of establishing a *prima facie* case of obviousness in regards to claims 1, 8, 12, 17, 20, 24 and 28, and, in addition, that claims 1, 8, 12, 17, 20, 24 and 28 as pending have been shown to be patentably distinct from the cited reference, either alone or in combination with the Examiner's taking of official notice or inherency. As claims 2-7, 9-11, 13-16, 18-19, 21-23, 25-27 and 29-30 depend from and further define claims 1, 8, 12, 17, 20, 24 and 28, respectively, they are also believed to be allowable. Accordingly, Applicant respectfully requests reconsideration and withdrawal of the rejection under 35 U.S.C. § 103(a) and allowance of claims 1-30.

CONCLUSION

If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2207.

Respectfully submitted,

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